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(54) Abstract Title
Lateral semiconductor device

(57)   A lateral Silicon-on-Insulator transistor 10 for high voltage applications. The SOI layer 15 has p+ source region 12 and n+ drain region 13. A drift region 14 is subdivided into uniformly doped p and n sub-regions 14', 14", extending laterally, forming a pn junction at the boundary which lies at an acute angle to a perpendicular drawn between the source and drain regions, giving trapezoidal/triangular sub-regions. When a reverse bias voltage is applied across the semiconductor layer 15, the n-type drift region 14" has an excess of charge relative to the p-type drift region 14' which varies linearly across the drift region 14, increasing towards the drain region 13. Greater uniformity of the electric field distribution is achieved, with elimination of peaks.

A MOSFET embodiment is described (figs 11, 12) having an extended gate, which forms a weak accumulation at the surface of the drift layer, reducing the resistance along the current path.
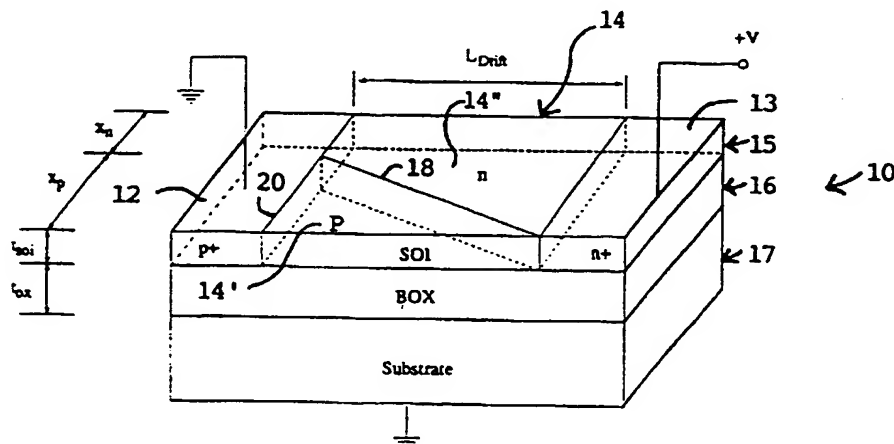
Figure 3

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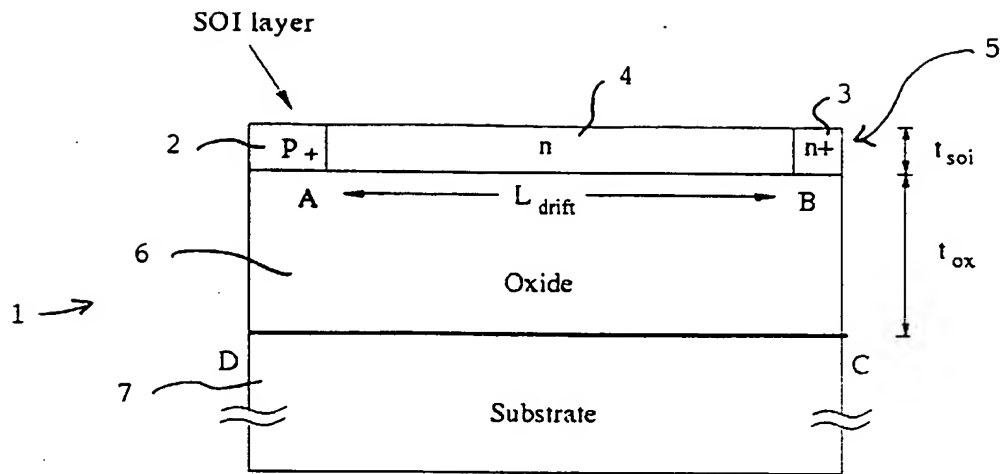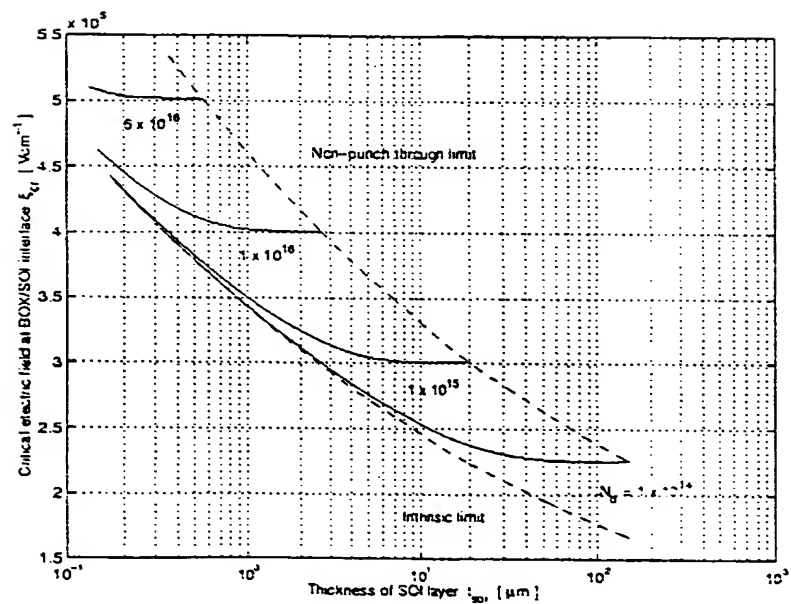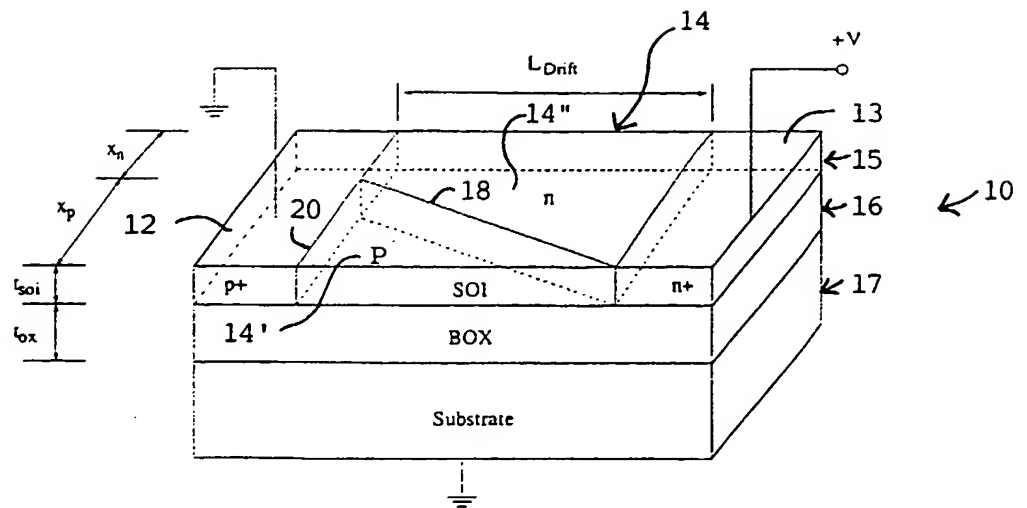At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

Figure 1

Figure 2

Figure 3
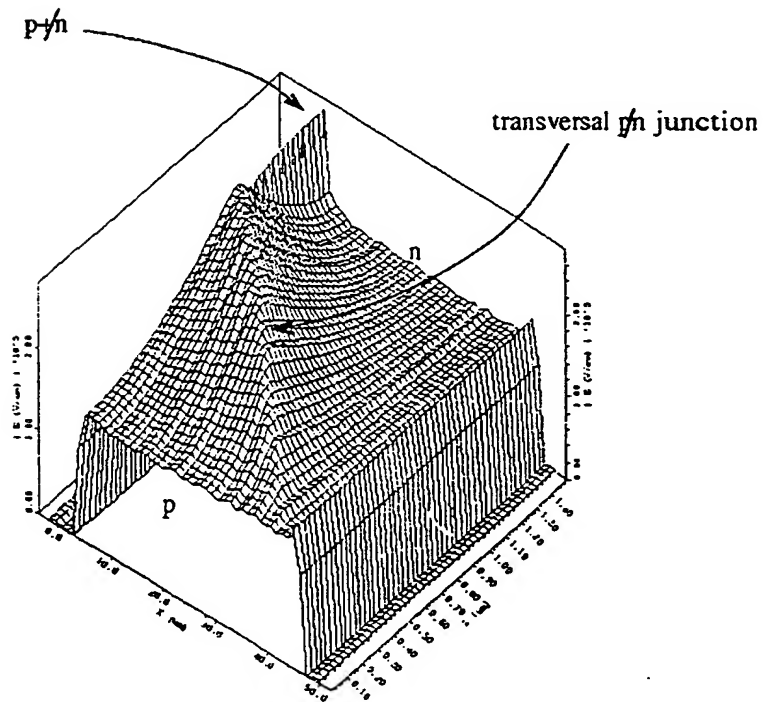
Figure 4
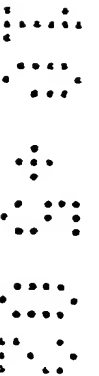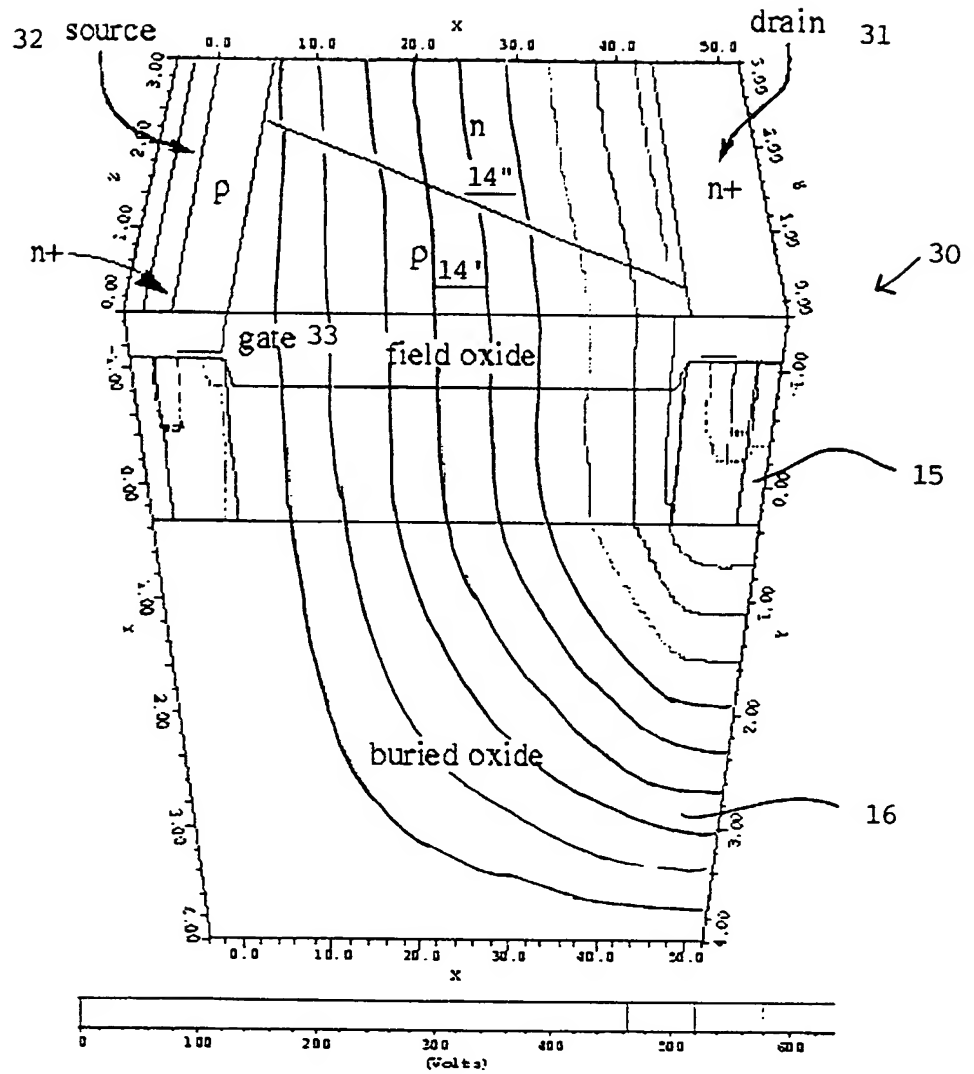
Figure 5
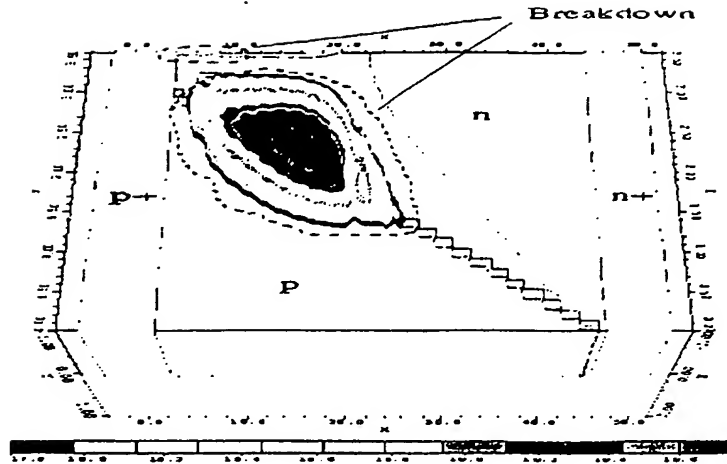
(a) Wide, p stripe $x_p = 3\mu m$ => breakdown voltage Vbr=261V
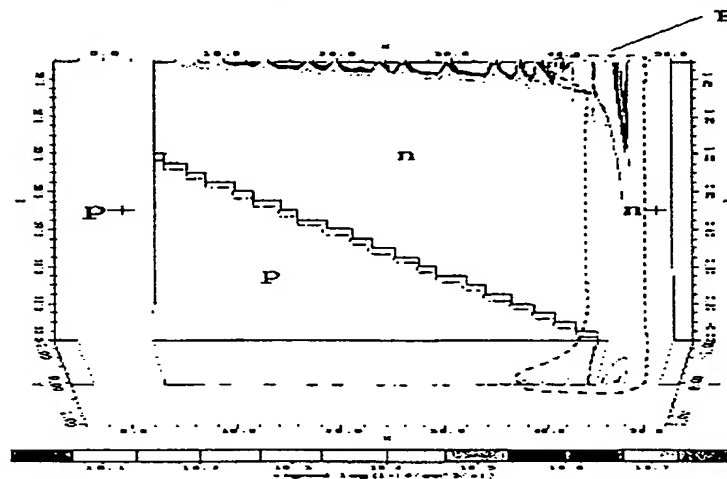
(b) Narrow, p stripe $x_p = 1\mu m$ => breakdown voltage Vbr=620V
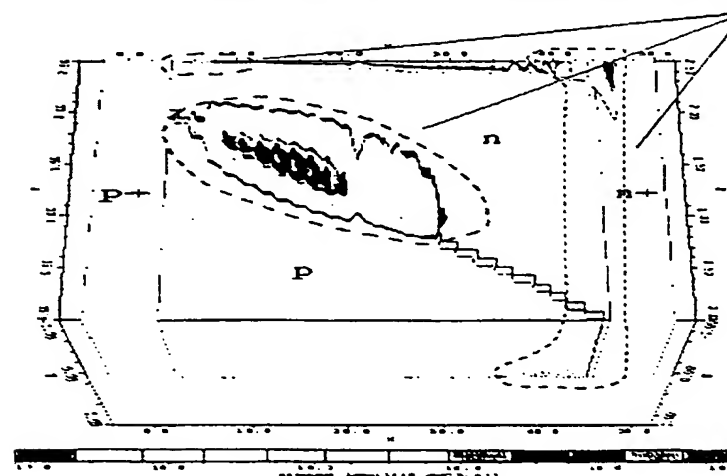
(c) Ideal, width $x_p = 2\mu m$ => breakdown voltage Vbr=615V

Figure 6
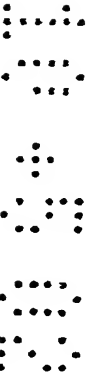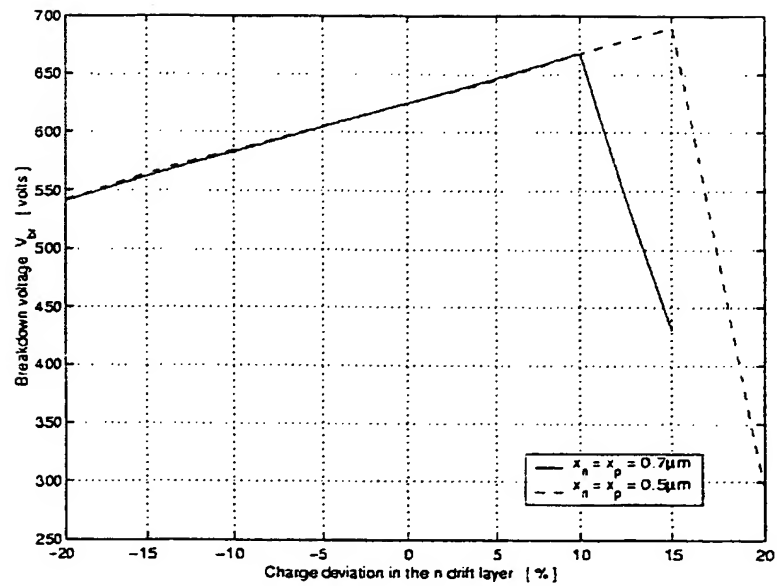
Figure 7
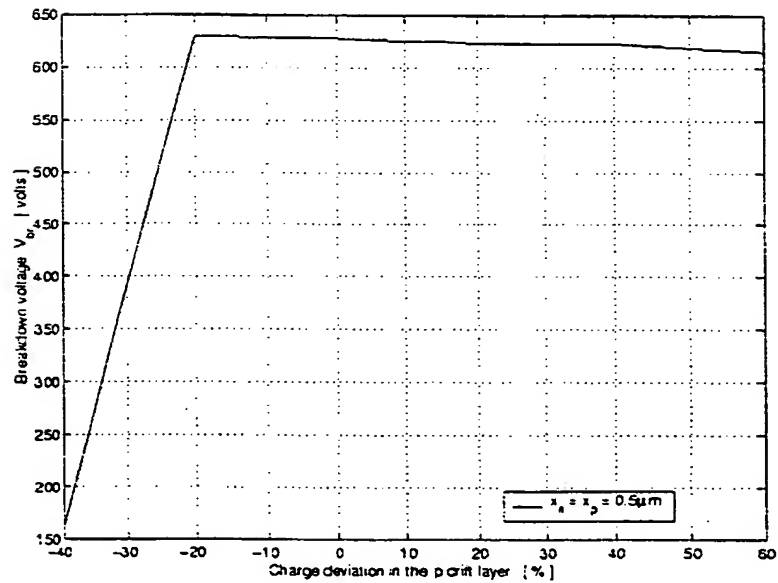
Figure 8

Figure 9

Figure 10

SOURCE   G133   DRAIN 31
32

34   14"

                                       15

                                       16

n

12   P   17

p+   n+   P
        p well   14' SOI   n well

36   35   BOX   37   13

30

Substrate

Figure 11

GATE1 (Field plate)   33   (Field plate)

34   n well 37

35

n+   2   3

p well   n   14"

1

SOURCE   4   n+   DRAIN 31

32   p+

P   14'

13

drift length

Figure 12

GATE1 (Field plate)   33

(Field plate)

34

n well   37

35

30

SOURCE
32

n+   p well   ②

②

n
③

14"

①

4

n+

DRAIN   31

P+

P

14'

13

drift length
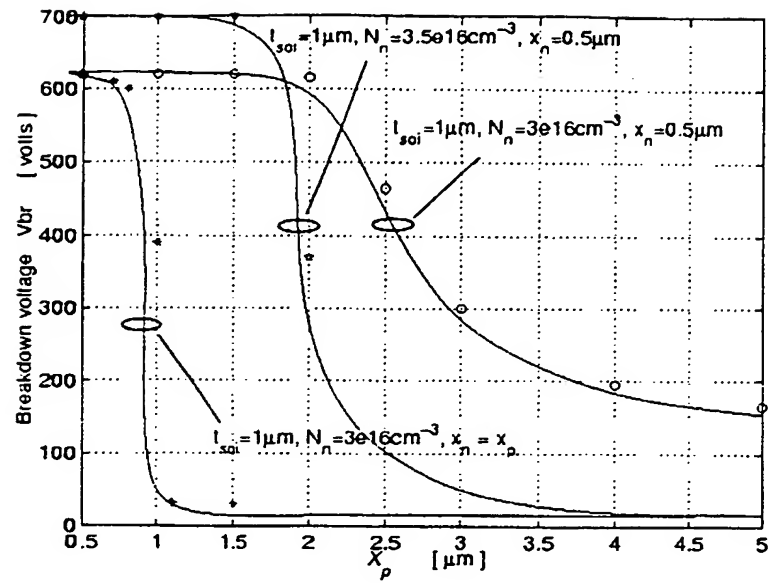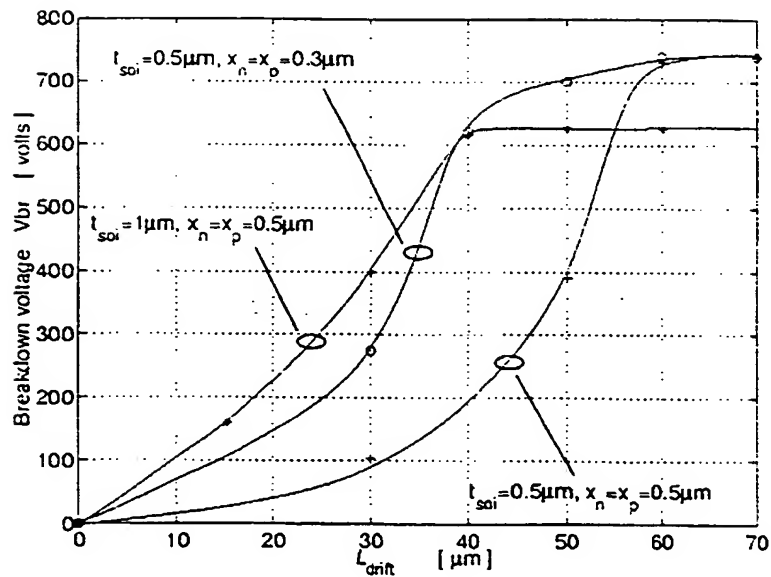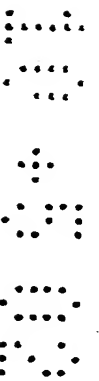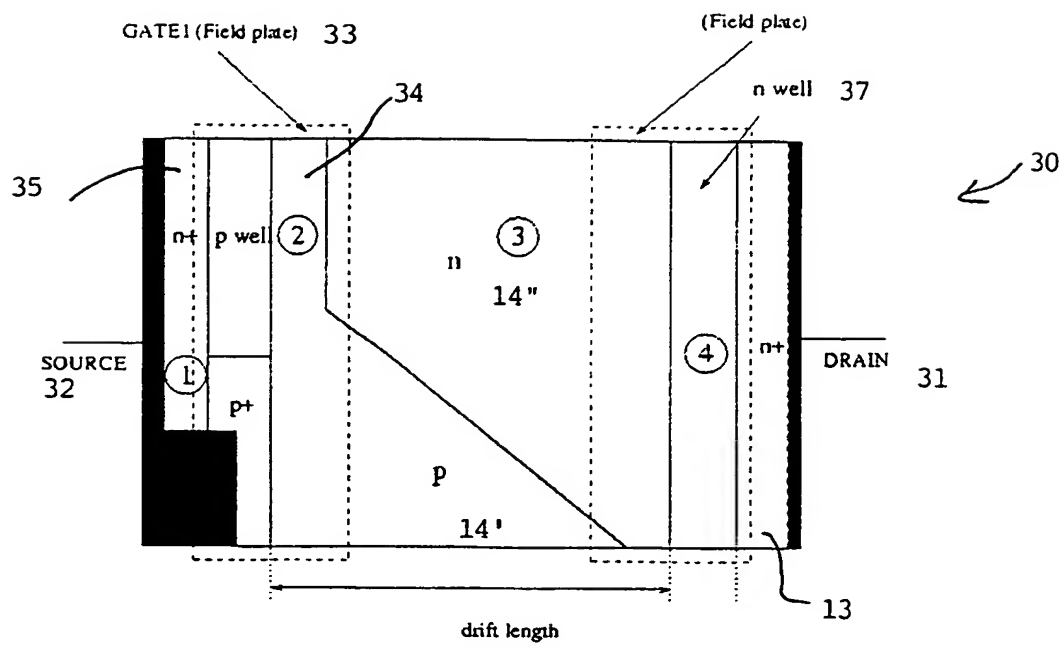
Figure 13
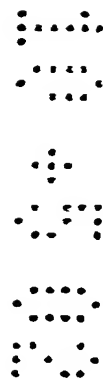
LATERAL SEMICONDUCTOR DEVICE

The present invention relates to a lateral
semiconductor device.

5

The present invention relates generally to the field
of high voltage semiconductor devices and more particularly
to high voltage lateral devices manufactured by the use of
SOI (Silicon-on-Insulator) technology.

10

As shown schematically in Figure 1, a typical lateral
high-voltage device 1 fabricated using SOI technology has a
basic configuration of a p+ region 2 and an n+ region 3 at
opposing ends separated by a central n drift region 4 of

15 lower conductivity, all of which are formed in an SOI layer
5 which is formed on an oxide layer 6 which itself is
formed on a silicon substrate 7. The p+ region 2 is
shorted to the substrate 7 below the BOX (buried oxide
layer) 6. In the blocking/off-state mode, a terminal (not

20 shown) connecting the p+ region 2 and the substrate 7 is
grounded and a high voltage reverse bias is applied to a
terminal (not shown) connected to the n+ region 3. As the
reverse bias is increased, a depletion layer develops
across the p+/n junction 2/4. The bulk of the depletion

25 layer forms within the central n region 4 so that a
significant portion of the applied reverse bias is
sustained inside the central n region 4. Simultaneously,
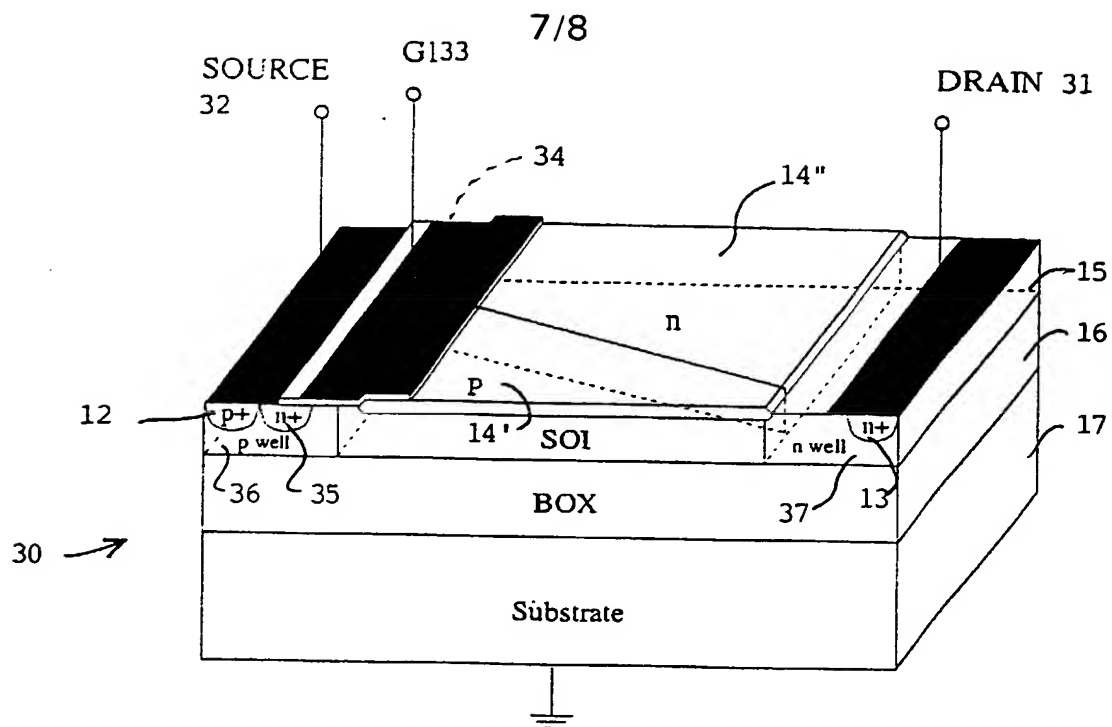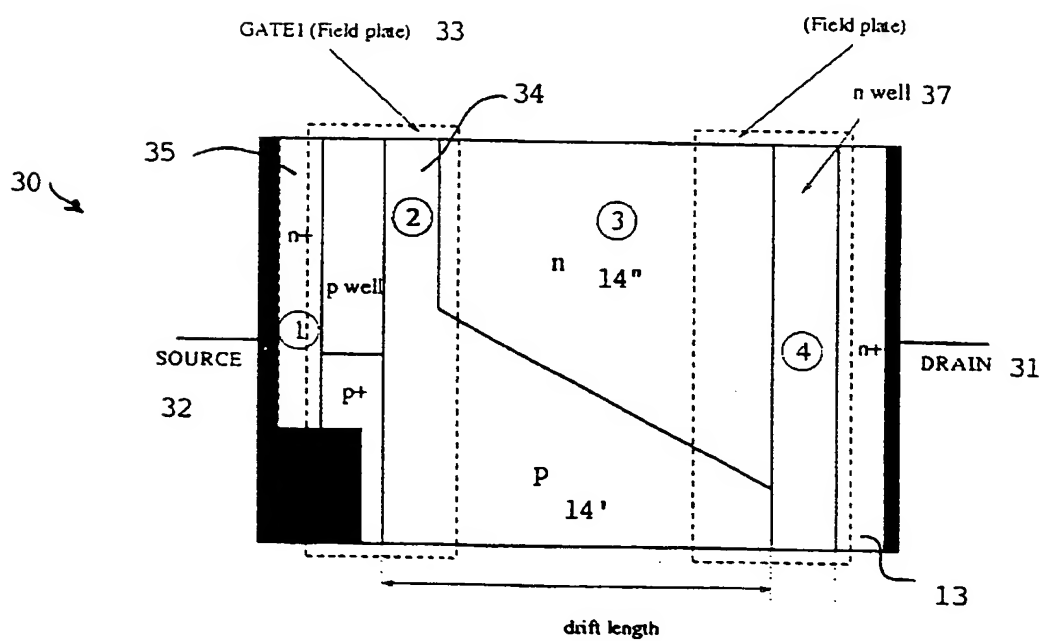due to a field effect action across the buried oxide 6, an
inversion/accumulation layer forms directly beneath the

30 buried oxide layer 6 in the p or n type substrate 7. This
layer of highly mobile charge maintains an equipotential
surface at ground potential beneath the buried oxide layer
6 and screens nearly all of the electric field from the

bulk of the substrate 7 and behaves in effect as a field plate. The field plate effect causes a crowding of the potential lines in the area surrounding the n+ region 3 which, during the blocking state, is connected to the

5 reverse bias. The electric field inside the depleted region of the central n region 4 is thus distorted and results in the formation of a second electric field peak near the n+ region 3 in addition to the original electric field peak occurring at the p+/n junction 2/4. This is the

10 so-called "RESURF" phenomenon observed in high voltage SOI devices. Unlike the RESURF effect in Junction Isolation (JI) technology, the RESURF effect in SOI is weak and this is mainly because the buried oxide layer 6 prevents a direct coupling of fixed ion charge between the substrate 7

15 and the upper SOI layer 5. The absence of this coupling excludes the formation of a depletion layer within the substrate 7. Thus, in such devices, the high voltage sustaining capability must come from either the SOI 5 or the buried oxide layer 6.

20

In the past, methods for achieving high blocking voltages have relied on a relatively thick SOI layer 5 to support the reverse bias. For instance, to reach 500 Volts, the SOI layer 5 should typically have a depth of 10

25 to 20µm. However, if for example a SOI layer 5 in excess of 5µm thickness is ruled out because of isolation problems, then the reverse bias must be supported almost entirely by the buried oxide layer 6.

30 Consider now the electric field at the SOI/BOX interface 5/6 for the device 1 in Figure 1. In the ideal case, the horizontal component of the electric field at

this interface will be constant, and the voltage along the line AB in Figure 1 will increase linearly towards B. Since the reverse bias is mainly supported by the oxide layer 6, it follows that the vertical component of the
5   electric field at the interface and within the oxide layer 6 must also increase linearly along AB. Thus, the main criterion for a perfect electric field distribution in SOI layers 5 of thin to medium thickness translates to the requirement of a vertical electric field ξy at the SOI/BOX
10   interface which is proportional to distance from the grounded end A.

One way of achieving this is by use of a thin linearly graded profile in the n drift region 4. Furthermore, if
15   the horizontal electric field distribution is constant, then any electric field due to the charge in the SOI layer 5 along a vertical line must terminate at the layer of mobile charges formed at the substrate/BOX interface 7/6. This allows the vertical electric field distribution along
20   any vertical line in the SOI layer 5 to be approximated as a triangular distribution. Another way of obtaining a linear distribution of the vertical electric field along the SOI/BOX interface 5/6 is via the use of a tapered or stepped buried oxide layer 6.
25

Referring again to Figurer 1, applying Gauss·'s law along the line BC at the high voltage end, the required distribution of the vertical electric field in the SOI layer 5 along the SOI/BOX interface 5/6 can be deduced as:

$$\xi_y(x) = \frac{\varepsilon_{ox} V_{br}}{\varepsilon_{si} t_{ox}} \left(\frac{x}{L_{drift}} \right)$$

30   (1)

and the corresponding doping profile is given by,

$$N_{SOI}(x) = \frac{\varepsilon_{ox} V_{br}}{q t_{soi} t_{ox}} \left(\frac{x}{L_{drift}} \right)$$

(2).

5   Because the electric field at the SOI/BOX interface 5/6 can be high, especially in high voltage devices, a thin SOI layer 5 must in practice be used as it allows a higher critical electric field to be sustained across it.   Figure 2 shows, for several doping concentrations, how the

10   critical electric field in silicon increases as the thickness of the silicon is reduced.

        S. Merchant, E. Arnold, S. Mukherjee, H. Pein and R. Pinker, "Realisation of High Breakdown Voltage (≤700 volts)

15   in Thin SOI Devices", ISPSD 91, p. 31 describe a previous attempt to achieve a uniform surface electric field distribution and exploit the voltage-supporting capability of the buried oxide by the use of a linearly graded doping profile in an ultra-thin (< 1μm) SOI layer.   In accordance

20   with equation (1) above, the doping profile increases from the grounded p+ region towards the n+ region connected to the reverse bias.   In another attempt to achieve greater uniformity of the electric field distribution, F. Udrea et al in "3D RESURF Double-Gate MOSFET: A revolutionary power

25   device concept", Electronic Letters, vol.34, no.8, April 1998, propose the use of parallel, alternating n and p stripes in the SOI region, in which the charge in the n stripe balances exactly the charge in the p stripe. However, use of charge-balanced, parallel n and p stripes

results in large electric field peaks at the n+ and p+ ends.

In practice, it is difficult to fabricate a device in
5   which the doping profile of any region varies uniformly linearly as required by these prior art proposals.

According to a first aspect of the present invention, there is provided a lateral semiconductor device, the
10 device comprising a semiconductor layer on an insulating layer on a semiconductor substrate, the semiconductor layer having a region of a first conduction type and a region of a second conduction type with a drift region therebetween, the drift region being provided by a region of the first
15 conduction type and a region of the second conduction type, the first and second conduction type drift regions being so arranged that when a reverse voltage bias is applied across the first and second conduction type regions of the semiconductor layer, the second conduction type drift
20 region has an excess of charge relative to the first conduction type drift region which varies substantially linearly from the end of the drift region towards the first conduction type region of the semiconductor layer to the end of the drift region towards the second conduction type
25 region of the semiconductor layer.

According to a second aspect of the present invention, there is provided a lateral semiconductor device, the device comprising a semiconductor layer on an insulating
30 layer on a semiconductor substrate, the semiconductor layer having a region of a first conduction type and a region of a second conduction type with a drift region therebetween,

the drift region being provided by a region of the first
conduction type and a region of the second conduction type,
a junction formed between the first and second conduction
type drift regions lying at an acute angle to a line
5 joining the first and second conduction type regions of the
semiconductor layer with a major portion of the first
conduction type drift region being towards the first
conduction type region of the semiconductor layer and a
major portion of the second conduction type drift region
10 being towards the second conduction type region of the
semiconductor layer, whereby when a reverse voltage bias is
applied across the first and second conduction type regions
of the semiconductor layer, the second conduction type
drift region has an excess of charge relative to the first
15 conduction type drift region which varies substantially
linearly from the end of the drift region towards the first
conduction type region of the semiconductor layer to the
end of the drift region towards the second conduction type
region of the semiconductor layer.

20

According to a third aspect of the present invention,
there is provided a lateral semiconductor device, the
device comprising a semiconductor layer on an insulating
layer on a semiconductor substrate, the semiconductor layer
25 having a region of a first conduction type and a region of
a second conduction type with a drift region therebetween,
the drift region being provided by a region of the first
conduction type and an adjacent region of the second
conduction type, the first and second conduction type drift
30 regions each being tapered with a major portion of the
first conduction type drift region being towards the first
conduction type region of the semiconductor layer and a
major portion of the second conduction type drift region

being towards the second conduction type region of the
semiconductor layer, whereby when a reverse voltage bias is
applied across the first and second conduction type regions
of the semiconductor layer, the second conduction type
5   drift region has an excess of charge relative to the first
conduction type drift region which varies substantially
linearly from the end of the drift region towards the first
conduction type region of the semiconductor layer to the
end of the drift region towards the second conduction type
10 region of the semiconductor layer.

The present invention provides a lateral semiconductor
device, which in the preferred embodiment is of the SOI
type, in which a high blocking voltage capability can be
15 achieved but without requiring a non-uniform doping profile
in any of the regions of the device. By providing (at
least) first and second conduction type drift regions, an
excess of charge can form in one of the first and second
conduction type drift regions relative to the other when a
20 reverse bias is applied across the device. In the
preferred embodiment, by appropriate arrangement of the
geometry of the first and second conduction type drift
regions, that excess of charge can effectively simulate the
non-uniform doping profile in the prior art proposal
25 discussed above, thus providing the desired increase in the
vertical electric field along the device discussed above.

The first conduction type drift region may be
substantially triangular or trapezoidal in shape parallel
30 to the plane of the device.

The second conduction type drift region may be substantially triangular or trapezoidal in shape parallel to the plane of the device.

5   The first conduction type drift region preferably has substantially uniform doping. The second conduction type drift region preferably has substantially uniform doping. Whilst not strictly necessary to achieve the desired excess charge and substantially linear variation along the device, 10 uniform doping profiles are much easier to fabricate controllably and reproducibly and are also easier to model than non-uniform doping profiles.

According to another aspect of the present invention, 15 there is provided a MOSFET comprising a semiconductor device as described above.

An embodiment of the present invention will now be described by way of example with reference to the 20 accompanying drawings, in which:

Figure 1 shows schematically a basic diode structure as used in known high-voltage SOI devices;

25   Figure 2 shows graphically the dependence of the critical electric field in the SOI layer on thickness t_{soi};

Figure 3 is a schematic perspective view of an example of a semiconductor device according to an embodiment of the 30 present invention;

Figure 4 shows schematically the electric field distributions at the surface of the SOI layer of the device of Figure 3 just before avalanche breakdown;

5   Figure 5 shows schematically the potential line distribution at a breakdown voltage V_{br}=620V in an example of a MOSFET according to an embodiment of the present invention;

10   Figures 6(a) to 6(c) show schematically impact ionisation generation rates indicating shift of position of avalanche failure respectively from the p+/n junction and p/n drift region junction, to the SOI/BOX interface, and to the p+/n junction and p/n drift region junction and the
15   SOI/BOX interface for optimised dimensions in which failure occurs throughout the bulk, for an example of a semiconductor device according to an embodiment of the present invention;

20   Figure 7 shows schematically the dependence of the breakdown voltage on the deviation of the n drift region charge/doping density as a percentage of $3x10^{16}cm^{-3}$ for an example of a semiconductor device according to an embodiment of the present invention;
25

Figure 8 shows schematically the dependence of the breakdown voltage on the deviation of the p drift region charge/doping density as a percentage of $3x10^{16}cm^{-3}$ for an example of a semiconductor device according to an
30   embodiment of the present invention;

Figure 9 shows graphically the influence of the initial width of the n and p drift regions on the breakdown voltage of an example of a diode according to an embodiment of the present invention;

5

Figure 10 shows graphically the influence of the drift length L_{drift} on the breakdown voltage of an example of a diode according to an embodiment of the present invention;

10   Figure 11 is a schematic perspective view of an example of a single gate MOSFET according to an embodiment of the present invention;

Figure 12 is a schematic plan view from above of the 15 MOSFET of Figure 11; and,

Figure 13 is a schematic plan view from above of another example of an n-channel single gate MOSFET according to an embodiment of the present invention.

20

Referring now to the drawings, Figure 3 shows schematically a perspective view of an example of a diode structure 10 according to a preferred embodiment of the present invention. A p+ region 12 and an n+ region 13 are 25 formed at opposed ends of the device 10 with a drift region 14 therebetween. The p+ region 12, n+ region 13 and drift region 14 are all formed in a semiconductor layer 15 which, in this example is silicon. The silicon layer 15 is itself formed on an insulating buried oxide layer (BOX) 16 which 30 itself is formed on a semiconductor substrate 17 which in this example is silicon, all as is known in SOI technology per se. Such a silicon layer 15 is conventionally referred to as the SOI layer 15. The drift region 14 in a practical

application of the present invention can form the drift regions and channel regions of a MOS-controllable device, as will be discussed further below.

5   The drift region 14 of this example is subdivided into two sub-regions 14',14". (In principle, it may be possible and even desirable to provide further sub-regions to the drift region 14.) The drift sub-regions 14',14" are so arranged such that when a reverse voltage bias is applied 10 across the p+ region 12 and n+ region 13, an excess of charge is formed in one of the drift sub-regions 14" relative to the other drift sub-region 14' and further such that this excess of charge varies substantially linearly with distance from the p+ region 12. As will be discussed 15 further below, this has the effect of ensuring that the vertical electric field at the SOI/BOX interface is proportional to the distance from the p+ region 12.

In the specific example shown in Figure 3, this 20 arrangement for the drift sub-regions 14',14" is achieved by the drift sub-regions 14',14" being of opposite conductivity type and arranged such that a junction 18 between the drift sub-regions 14',14" lies at an acute angle to a line joining the p+ region 12 and the n+ region 25 13. The drift sub-regions 14',14" therefore effectively taper and when viewed from above typically have a generally triangular or trapezoidal shape. As shown in Figure 3, the n drift sub-region 14" is orientated with its major portion or wide end 19 positioned towards the n+ region 13. 30 Similarly, the major portion or wide end 20 of the p drift sub-region 14' is towards the p+ region 12. Each of the p and n drift sub-regions 14',14" preferably has a uniform doping profile.

As in a normal p/n junction, the p and n drift sub-
regions 14',14" initially deplete transversely along the
junction 18 on application of a reverse bias. However, due
5 to the geometry of the drift sub-regions 14',14", the total
charge in the p drift sub-region 14' is considerably less
than that in the n drift sub-region 14". This compensates
for the extra charge in the inversion layer below the
buried oxide layer 16. By approximating the depletion of
10 the p and n drift sub-regions 14',14" as a one-dimensional
p/n junction, it can be seen that less and less charge in
the n drift sub-region 14" is balanced out by the charge in
the p drift sub-region 14' on progression from the grounded
p+ region 12 to the n+ region 13. As will be understood,
15 the effective charge/doping concentration in the SOI layer
15 once the p drift sub-region 14' is fully depleted is
simply:

$$N_{n_{eff}}(x) = \frac{x_n - x_p}{L_{drift}} N_n$$

(3)

20

This in effect simulates a linearly graded doping
profile and gives the desired linearly graded charge
profile. Therefore, to achieve the ideal electric field
25 distribution, it is necessary only to adjust the variables
in the expression (3) so that it matches the expression (2)
discussed above.

The main parameters that affect the breakdown voltage
30 in such devices are (i) the thickness t_{SOI} of the SOI layer
15, (ii) the doping concentration N_n of the n drift sub-

region 14", (iii) the initial width X_n, X_p of both the n and p drift sub-regions 14",14' as measured at the p+ region 12 end, and (iv) the length L_{drift} of the drift region 14.

5   The first and most important parameter, the thickness t_{soi} of the SOI layer 15, has already been discussed above. It is found that in order to support high voltages in the oxide layer 16, a thin SOI layer 15 should be employed.

10   The second parameter determines the electric field enhancement at the SOI/BOX layer interface. From Figure 2, it can be seen that increasing the doping concentration results in a larger critical electric field at the interface as compared to the case when the doping 15 concentration in the SOI layer 15 is at the intrinsic level. The upper limit to which the doping concentration can be raised is dictated by the thickness t_{soi} of the SOI layer 15.

20   The third variable, which is the initial width of both the n and p drift sub-regions 14",14', in each case should not exceed a critical value determined by the doping concentrations of the n and p drift sub-regions 14",14' and especially that of the n drift sub-region 14". This is 25 necessary to suppress breakdown across the oblique p/n junction 18 and to ensure full transversal depletion of the p and n drift sub-regions 14',14". The surface electric field distribution shown in Figure 4 plotted just before breakdown for the device 10 of Figure 3 indicates electric 30 field peaks at (a) the corner of the p+/n junction 12/14" and (b) the portion of the p/n junction 18 nearer the p+ region 12. Additionally, as shown in Figure 5 for an example of a MOSFET according to the present invention,

potential lines crowding near the high voltage terminal 31
generate a large electric field at the SOI/BOX interface
15/16.   Breakdown can initiate at any of these places.   If
the initial widths or doping concentrations of the n and p
5   drift sub-regions 14",14' are too large, early breakdown
occurs on the surface at the p+/n corner 12/14" and across
the oblique p/n junction 18 as indicated by the impact
ionisation generation rates shown in Figure 6(a).   By
reducing the widths, breakdown can be shifted to the
10   SOI/BOX interface 15/16 as shown in Figure 6(b).   In the
optimised structure, avalanche occurs simultaneously at the
p+/n junction 12/14", the oblique p/n junction 18 on the
surface, and the SOI/BOX interface 15/16, as shown in
Figure 6(c).

15

   The effect of charge imbalance in the n and p drift
sub-regions 14",14' on the breakdown of the device 10 is
shown in Figures 7 and 8 respectively for the case where
$L_{drift}=40\mu m$, $t_{soi}=1\mu m$, $t_{ox}=4\mu m$ and $x_n, x_p =0.5\mu m$.   Figure 9
20   shows the influence of the initial width x_n, x_p of the drift
sub-regions 14",14' on the breakdown voltage for $L_{drift}=40\mu m$,
$t_{soi}=1\mu m$, $t_{ox}=4\mu m$ and $N_n=3\times10^{16}cm^{-3}$.   Figure 10 shows the
variation of breakdown voltage with drift length L_{drift} for
$t_{ox}=4\mu m$ and the cases of $N_n=3\times10^{16}cm^{-3}$ for $t_{soi}=1\mu m$ and
25   $N_n=7\times10^{16}cm^{-3}$ for $t_{soi}=0.5\mu m$.

   In summary, the fundamental requirement for a near
uniform electric field distribution is that the vertical
component of the electric field at the SOI/BOX interface
30   increases proportionally with distance from the grounded
end.   Previously to achieve such an electric field
distribution, a linearly graded profile was employed.   In

accordance with the preferred embodiment of the present invention, it will be recognised that the linearly graded profile can be dispensed with and the same effect achieved using uniform doping profiles by producing an effective

5 charge/doping concentration in the SOI layer which increases linearly. In the preferred embodiment, the effective charge in the n drift region is varied by varying the width of both the p and n drift sub-regions from the p+ region connected to the low voltage terminal end to the n+

10 region connected to the reverse bias. To compensate for the effect of the mobile charge layer under the buried oxide, the n drift sub-region widens towards the high voltage terminal end whereas the p drift sub-region becomes narrower. In the preferred embodiment, this is achieved

15 through the use of triangularly or trapezoidal shaped n and p drift sub-regions.

Figures 11 and 12 show schematically an n-channel single gate MOSFET 30 having trapezoidal p and n drift sub-

20 regions 14',14". Similarly a single gate MOSFET having a triangular p drift sub-region 14' is shown schematically in Figure 13. P-channel devices can be built by exchanging the positions of all the n and p type regions, as will be well understood.

25

In order to form a MOSFET, a MOSFET channel must be formed at the surface of the device. This can be accomplished by replacing part of the p+ region 12 of the device 10 shown in Figure 3 with a p layer 34 just before

30 the n drift sub-region 14" as shown schematically in Figures 11, 12 and 13. The usual n+ source 35 and p well 36 at the source end and the n well 37 at the drain end are also provided. In the forward blocking state, the

interaction between the p/n junctions and the layer of
mobile charge is similar to that described above. In the
on state, the p layer 34 (region 2 in Figures 11 to 13) can
be inverted by applying a potential higher than the

5   threshold voltage to the MOSFET gate (G1) 33. Electrons
will then flow from the n+ source 35 (region 1) through the
channel formed in the p layer 34 (region 2), n drift sub-
region 14" (region 3) to the drain region 13,37 (region 4)
and the drain terminal 31.

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To increase the conductivity of the drift region 14,
the MOSFET gate (G1) 33 in the single gate version
discussed above can be extended. The extended gate serves
two distinct functions. In the blocking state, the

15   extended gate is usually held at the same potential as the
p region source end. Under this condition, the extended
gate acts as a field plate much like the layer of mobile
charge in the substrate beneath the buried oxide layer. By
symmetry, either the doping concentrations in the p and n

20   drift sub-regions are raised by almost a factor of two and
the thickness of the SOI layer remains unchanged, or the
doping concentrations in the p and n drift sub-regions
remain unchanged but the thickness of the SOI layer is
increased. In the on state, the extended portion of the

25   gate forms a weak accumulation/inversion at the surface of
the n/p drift sub-region layer. This helps to reduce the
resistance along the current path.

There has thus been disclosed a technique for
30   achieving high breakdown voltages on thin SOI layers (<3μm)
with a moderately thick buried oxide layer (≤4μm) and which
allow a uniform doping profile to be used. In the

preferred embodiment, this is provided for by a structure
having three main lateral junctions, two of which are
parallel to each other and transverse to the line joining
the p+ and n+ regions 12,13 in the SOI layer 15 and the

5 third of which connects the other two and is at an acute
angle thereto, each junction being formed in the SOI layer
15.   Together with the mobile charge layer beneath the
buried oxide layer 16, the parallel and transverse
junctions realise a uniform distribution of the electric

10 field in the off state.

An embodiment of the present invention has been
described with particular reference to the examples
illustrated.   However, it will be appreciated that

15 variations and modifications may be made to the examples
described within the scope of the present invention.   For
example, whilst the junction 18 between the p and n drift
sub-regions 14',14" is linear in the examples described
above, the junction 18 may have another configuration,

20 including for example curved or flared.   In addition, the
abutting edges of the p and n drift sub-regions 14',14" at
the junction 18 need may have a shape such as stepped or
serpentine or may have some irregular shape.

CLAIMS

1. A lateral semiconductor device, the device comprising
a semiconductor layer on an insulating layer on a
5   semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
conduction type with a drift region therebetween, the drift
region being provided by a region of the first conduction
type and a region of the second conduction type, the first
10 and second conduction type drift regions being so arranged
that when a reverse voltage bias is applied across the
first and second conduction type regions of the
semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first
15 conduction type drift region which varies substantially
linearly from the end of the drift region towards the first
conduction type region of the semiconductor layer to the
end of the drift region towards the second conduction type
region of the semiconductor layer.

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2. A lateral semiconductor device, the device comprising
a semiconductor layer on an insulating layer on a
semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
25 conduction type with a drift region therebetween, the drift
region being provided by a region of the first conduction
type and a region of the second conduction type, a junction
formed between the first and second conduction type drift
regions lying at an acute angle to a line joining the first
30 and second conduction type regions of the semiconductor
layer with a major portion of the first conduction type
drift region being towards the first conduction type region
of the semiconductor layer and a major portion of the

second conduction type drift region being towards the
second conduction type region of the semiconductor layer,
whereby when a reverse voltage bias is applied across the
first and second conduction type regions of the
5   semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first
conduction type drift region which varies substantially
linearly from the end of the drift region towards the first
conduction type region of the semiconductor layer to the
10   end of the drift region towards the second conduction type
region of the semiconductor layer.

3.   A lateral semiconductor device, the device comprising
a semiconductor layer on an insulating layer on a
15   semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
conduction type with a drift region therebetween, the drift
region being provided by a region of the first conduction
type and an adjacent region of the second conduction type,
20   the first and second conduction type drift regions each
being tapered with a major portion of the first conduction
type drift region being towards the first conduction type
region of the semiconductor layer and a major portion of
the second conduction type drift region being towards the
25   second conduction type region of the semiconductor layer,
whereby when a reverse voltage bias is applied across the
first and second conduction type regions of the
semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first
30   conduction type drift region which varies substantially
linearly from the end of the drift region towards the first
conduction type region of the semiconductor layer to the

end of the drift region towards the second conduction type
region of the semiconductor layer.

4.   A lateral semiconductor device according to any of
claims 1 to 3, wherein the first conduction type drift
region is substantially triangular or trapezoidal in shape
parallel to the plane of the device.

5.   A lateral semiconductor device according to any of
claims 1 to 4, wherein the second conduction type drift
region is substantially triangular or trapezoidal in shape
parallel to the plane of the device.

6.   A lateral semiconductor device according to any of
claims 1 to 5, wherein the first conduction type drift
region has substantially uniform doping.

7.   A lateral semiconductor device according to any of
claims 1 to 6, wherein the second conduction type drift
region has substantially uniform doping.

8.   A MOSFET comprising a semiconductor device according
to any of claims 1 to 7.

9.   A lateral semiconductor device substantially in
accordance with any of the examples as hereinbefore
described with reference to and as illustrated by Figures 2
to 13 of the accompanying drawings.

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CLAIMS

1.   A lateral semiconductor device, the device comprising
a semiconductor layer on an insulating layer on a
5   semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
conduction type with a drift region therebetween, the drift
region being provided by a region of the first conduction
type and a region of the second conduction type, the first
10   and second conduction type drift regions being so arranged
that when a reverse voltage bias is applied across the
first and second conduction type regions of the
semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first
15   conduction type drift region that increases substantially
linearly from the end of the drift region that is towards
the first conduction type region of the semiconductor layer
to the end of the drift region that is towards the second
conduction type region of the semiconductor layer and such
20   that the total charge in the second conduction type drift
region is greater than the total charge in the first
conduction type drift region.

2.   A lateral semiconductor device, the device comprising
25   a semiconductor layer on an insulating layer on a
semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
conduction type with a drift region therebetween, the drift
region being provided by a region of the first conduction
30   type and a region of the second conduction type, a junction
formed between the first and second conduction type drift
regions lying at an acute angle to a line joining the first
and second conduction type regions of the semiconductor

layer with a major portion of the first conduction type
drift region being towards the first conduction type region
of the semiconductor layer and a major portion of the
second conduction type drift region being towards the

5   second conduction type region of the semiconductor layer,
whereby when a reverse voltage bias is applied across the
first and second conduction type regions of the
semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first

10   conduction type drift region that increases substantially
linearly from the end of the drift region that is towards
the first conduction type region of the semiconductor layer
to the end of the drift region that is towards the second
conduction type region of the semiconductor layer, the

15   first and second conduction type drift regions being
arranged such that the total charge in the second
conduction type drift region is greater than the total
charge in the first conduction type drift region.

20   3.   A lateral semiconductor device, the device comprising
a semiconductor layer on an insulating layer on a
semiconductor substrate, the semiconductor layer having a
region of a first conduction type and a region of a second
conduction type with a drift region therebetween, the drift

25   region being provided by a region of the first conduction
type and an adjacent region of the second conduction type,
the first and second conduction type drift regions each
being tapered with a major portion of the first conduction
type drift region being towards the first conduction type

30   region of the semiconductor layer and a major portion of
the second conduction type drift region being towards the
second conduction type region of the semiconductor layer,
whereby when a reverse voltage bias is applied across the

first and second conduction type regions of the
semiconductor layer, the second conduction type drift
region has an excess of charge relative to the first
conduction type drift region that increases substantially

5 linearly from the end of the drift region that is towards
the first conduction type region of the semiconductor layer
to the end of the drift region that is towards the second
conduction type region of the semiconductor layer, the
first and second conduction type drift regions being

10 arranged such that the total charge in the second
conduction type drift region is greater than the total
charge in the first conduction type drift region.

4.   A lateral semiconductor device according to any of

15 claims 1 to 3, wherein the first conduction type drift
region is substantially triangular or trapezoidal in shape
parallel to the plane of the device.

5.   A lateral semiconductor device according to any of

20 claims 1 to 4, wherein the second conduction type drift
region is substantially triangular or trapezoidal in shape
parallel to the plane of the device.

6.   A lateral semiconductor device according to any of

25 claims 1 to 5, wherein the first conduction type drift
region has substantially uniform doping.

7.   A lateral semiconductor device according to any of
claims 1 to 6, wherein the second conduction type drift

30 region has substantially uniform doping.

8.   A MOSFET comprising a semiconductor device according
to any of claims 1 to 7.

9.   A lateral semiconductor device substantially in accordance with any of the examples as hereinbefore described with reference to and as illustrated by Figures 2 to 13 of the accompanying drawings.

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Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
X	1-8	US6023090	(PHILIPS ELECTRONICS) fig 4, col 4 lines 19-32
X	1-8	US5438215	(SIEMENS) fig 7, col 4 lines 5-29
X	1	US6127703	(PHILIPS ELECTRONICS) fig 2, col 3 lines 23-41
X	1	JP8316469	(TOKYO SHIBAURA ELECTRIC) English language abstract, fig

Categories:

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Field of Search:

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Worldwide search of patent documents classified in the following areas of the IPC^7:

H01L

The following online and other databases have been used in the preparation of this search report:

EPODOC, WPI, JAPIO